

Multi-Chip Implementation of a Biomimetic VLSI Vision Sensor Based on the Adelson-Bergen Algorithm

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Abstract. Biological motion sensors found in the retinas of species ranging from flies to primates are tuned to specific spatio-temporal frequencies to determine the local motion vectors in their visual field and perform complex motion computations. In this study, we present a novel implementation of a silicon retina based on the Adelson-Bergen spatio-temporal energy model of primate cortical cells. By employing a multi-chip strategy, we successfully implemented the model without much sacrifice of the fill factor of the photoreceptors in the front-end chip. In addition, the characterization results proved that this spatio-temporal frequency tuned silicon retina can detect the direction of motion of a sinusoidal input grating down to 10 percent contrast, and over more than a magnitude in velocity. This multi-chip biomimetic vision sensor will allow complex visual motion computations to be performed in real-time.

1 Introduction

Every organism in nature must struggle to survive within its perceived truth by the help of its senses. What organisms perceive is only a noisy flow of sensation and this does not necessarily represent the perfect truth of their environment, but in fact provides information on their indispensable sensed truth. The biological strategies they have adopted have been proven to be effective and reliable by evolution. In this respect, when building artificial vision systems these biological models can be taken as a reference to deal with real life tasks such as target tracking and object avoidance. These systems employ massively parallel processing in dealing with complex and dynamic visual tasks and by incorporating the same strategy with parallel VLSI design principles in artificial systems, reliable low-power real-time neuromorphic systems can be built.

In this study we present a multi-chip system implementation of an analog VLSI hardware visual motion sensor based on the Adelson-Bergen motion energy model [1]. The Adelson-Bergen spatiotemporal energy model is a biological model and is often used as a model to describe primate cortical complex cells [2],[3]. In addition, it is classified under the correlation-based algorithms which are utilized to explain the optomotor response in flies [4] and direction selectivity in a rabbit's retina [5].

Multi-chip implementations are very suitable especially to achieve 2D optical flow motion computation [8]. These kind of systems integrate analog circuitry with an asynchronous digital interchip communication which is based on the Address-Event Representation (AER) protocol proposed by Mahowald [9] and revised by Boahen [13]. We utilized the same protocol in our implementation of the Adelson-Bergen algorithm to achieve the communication between sender and receiver chips.

A software version of the Adelson-Bergen algorithm was implemented on general-purpose analog neural computer by Etienne-Cummings [6]. Later, Higgins and Korrapati [7] implemented a monolithic analog VLSI sensor based on this algorithm. The main reason why we employed the Adelson-Bergen algorithm in motion computation is that it responds to real-world stimuli better than other algorithms and is therefore more amenable for robotic applications. Here we show that by incorporating the advantages of the model with a modular strategy the computational overload in the front-end chip can be reduced noticeably and the fill factor of the photoreceptors can be kept high. In addition the analog hardware implementation of the model exploits the subthreshold behavior of MOS transistors and therefore consumes little power. Furthermore, it works in real time, adapts to its environment and utilizes a massively parallel processing biological strategy by aligning in parallel arrays in the silicon retina.

2 Algorithm

The Adelson-Bergen algorithm is a spatiotemporal frequency tuned algorithm which obtains its direction selectivity by integrating quadrature filters with a nonlinearity. This algorithm is used in motion computation to extract the Fourier energy in a band of spatiotemporal frequencies regardless of phase of the stimulus. In this study, the Adelson-Bergen algorithm has been implemented (in a modified form; see Figure-1) by making use of Neuromorphic principles [10] and simplified without modifying the basic idea of spatiotemporal energy model.

Firstly, the spatial filtering in the model is trivialized by simply taking photoreceptor outputs separated by a $\Delta\Phi$ spatial distance between adjacent photoreceptors. Secondly, temporal filters in the model are implemented by employing an integrating circuit. Here we demonstrate that the integrating receiver circuitry can be used to attain a phase difference close to 90 degrees. This novel technique of using an integrator instead of a low-pass filter as a temporal filter enables us to exploit the advantages of multi-chip strategy in motion computation and to decrease the computational overload. Finally, the nonlinearity required to realize the algorithm is attained in the implementation by making use of the mathematical properties of rectification.

3 Hardware Architecture

In this section, the hardware architecture of the Adelson-Bergen algorithm is explained in detail. The overall organization of the multi-chip system is illus-

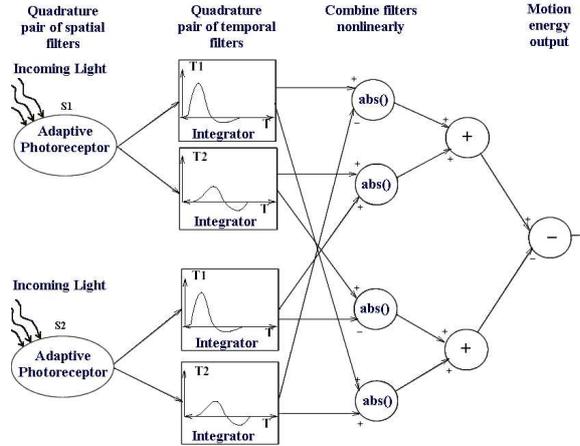


Fig. 1. Modified Adelson-Bergen spatiotemporal energy model

trated in Figure-2. The system consists of two chips, namely sender and receiver chips. These chips communicate by using the AER protocol [13] (Figure-4a) and perform all computations in current mode to minimize the space and maximize the fill-factor of the front-end chip.

In this implementation, the sender chip is employed to sense the intensity changes in the environment with respect to its adapted background and send this information to the receiver chip. It includes an array of pixels that discretize space and incorporates a photoreceptor, transconductance amplifier, rectifier and AER interface circuitry. In order to sense the intensity changes in the environment we used adaptive photoreceptors (Figure-3a) by Liu [11]. This photoreceptor provides a continuous-time signal that has a low gain for static signals and a high gain for transient signals. In addition to the photoreceptor output, an internal feedback voltage in this circuit is utilized in the motion computation to obtain information on the change of the adapted background level of its environment. This feedback voltage represents the running average of the illumination level of the background and the time interval of the averaging operation can be changed by altering the adaptation time. In the next stage, the response of the photoreceptor is compared with its feedback voltage and converted to current by making use of a transconductance amplifier shown in Figure-3b. In this way, we obtain a bandpass characteristic from the photoreceptor and transconductance amplifier pair. This characteristic ensures that very high frequencies are attenuated and offset or in this case the background level, is removed. After that, the output current of the transconductance amplifier is rectified by utilizing a full-wave rectifier (Figure-3c) in order to acquire separate currents for negative and positive intensity changes. Lastly, the communication interface circuitry that sends these intensity changes to the corresponding pixels

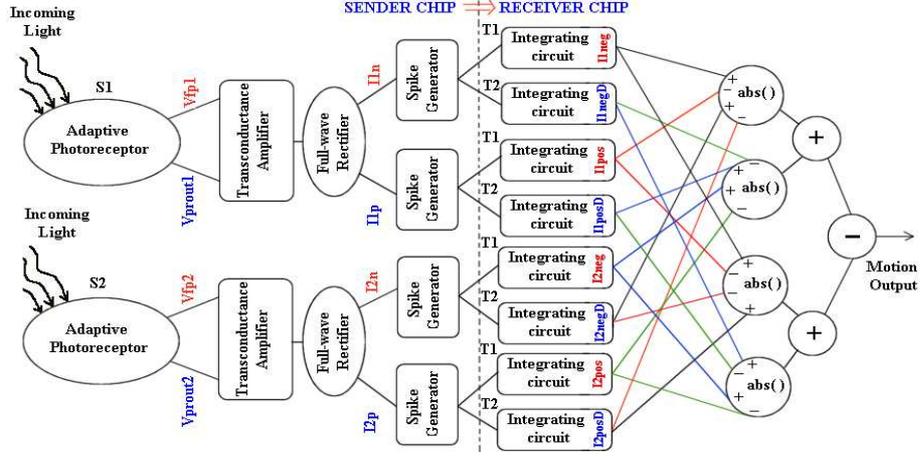


Fig. 2. The multi-chip implementation of the Adelson-Bergen algorithm. V_{prouT} and V_{fb} represent the photoreceptor's output and feedback response, respectively. In addition, I_p and I_n refer to positive and negative parts of the rectified signal, and in the receiver part, I_{pos} and I_{neg} represent the integrated versions of these signals. Lastly, I_{posD} and I_{negD} are the signals that are delayed relative to I_{pos} and I_{neg} .

in the receiver chip is implemented. This interface circuitry generates spikes with a frequency proportional to the amplitude level of the intensity change.

The receiver chip is utilized to achieve small field motion computation by making use of the information obtained from the sender chip. It is composed of the AER communication circuitry and corresponding pixels of the sender chip. In this implementation, the integrating circuit is employed not only to integrate the incoming spikes but also to attain necessary delays. The integrating receiver circuit has a particular spike frequency f_0 for which the charging and discharging current are the same on average keeping output voltage at a steady state value. In Figure-4c, the relationship between the voltage output and incoming spike frequency is illustrated. Similar to low-pass characteristics, this circuit can be incorporated to obtain the necessary delay and is therefore amenable to be used as a temporal filter. Accordingly, the positive or negative part of the signal is integrated by two integrating circuits tuned to different temporal frequencies in order to obtain a similar configuration as it was achieved with monolithic implementation [7]. As a result, the integrated positive and negative parts of the signal are summed, subtracted and absolute valued to perform the motion computation illustrated in Figure-2. The formulation of the final output is shown below.

$$I_{out} = |I_{1neg} + I_{2negD} - I_{1pos} - I_{2posD}| + |I_{2neg} + I_{1posD} - I_{1negD} - I_{2pos}| - |I_{1neg} + I_{2posD} - I_{1pos} - I_{2negD}| - |I_{2neg} + I_{1negD} - I_{2pos} - I_{1posD}| \quad (1)$$

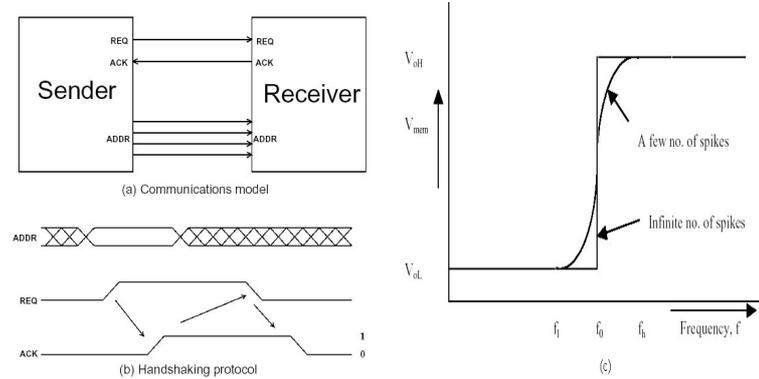


Fig. 4. AER protocol summary. (a) The model for AER transmission: a sender chip communicates with a receiver chip via request, acknowledge and address lines. (b) The handshaking protocol for transmission using the control and address lines: a request with a valid address leads to an acknowledgment, which in turn leads to falling request and falling acknowledge. (c) V_{out} vs. frequency sketch.

is obvious from the graph that the model responds best to a particular spatiotemporal frequency for which it is tuned and the response decreases at other frequencies.

5 Discussion

We have described and characterized a novel spatiotemporal frequency tuned multi-chip analog VLSI motion sensor and presented a new technique to realize the temporal filters needed for motion computation. The characterization results clearly elucidate the fact that by using this technique, we can obtain a reliable, low-power and real time multi-chip Neuromorphic motion processing system while retaining many of the advantages of monolithic implementation.

The multi-chip sensor responds to optimal spatial frequencies over a velocity range of more than an order of magnitude. Since the motion sensor is tuned to spatiotemporal frequencies, the main concern is to increase the range of the spatial and temporal frequencies and the contrast level to which it can respond. As seen from the spatiotemporal plot (Figure-6c), the response range of the multi-chip motion sensor is increased in comparison to monolithic implementation by Higgins and Korrapati [7]. The area of this region increased two times compared to the monolithic implementation. Besides, the immunity of the sensor to low contrast levels is improved. These results clearly indicate the improvement in the performance while the motion computation capability of the system is vastly increased compared to any space limited monolithic system. Furthermore, 2D motion computation can be easily achieved with this implementation by using a single sender chip with two two receivers and manipulating the x and y connections of the address lines of the second receiver.

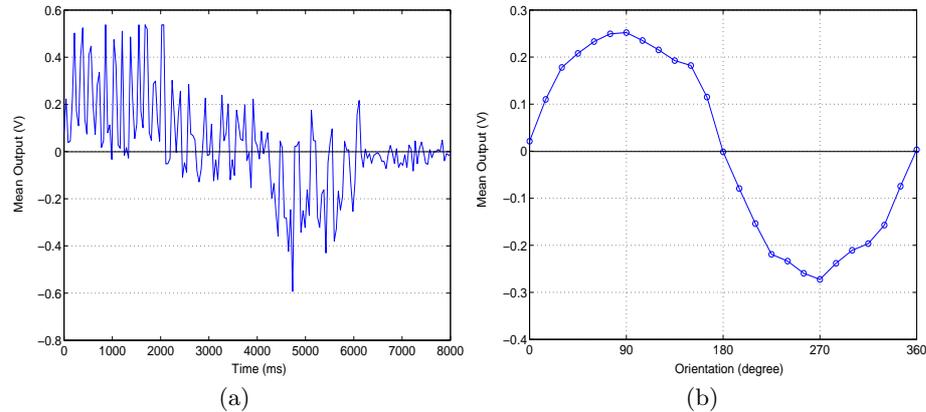


Fig. 5. (a) Output of the motion sensor. In the interval 0-2 seconds, a preferred direction sinusoidal stimulus is presented. Between 2-4 seconds, a sinusoidal stimulus moving orthogonal to the sensor orientation is presented. After that, sensor is exposed to a null direction sinusoidal stimulus. Lastly, no stimulus is presented between 6-8 seconds. (b) Orientation sweep. A sinusoidal stimulus is presented at varying directions relative to the motion sensor, which is optimally oriented for a stimulus at 90 degrees.

By using a multi-chip system, we obtained 36 pixels in a standard $1.5\mu\text{m}$ CMOS process and 2mm-by-2mm die size. In a new designed sender chip, positive and negative parts of the rectified signal will be sent through with a novel technique implemented in the AER system. With this implementation, we are expecting to exceed the number of pixels that can currently be realized on a single chip.

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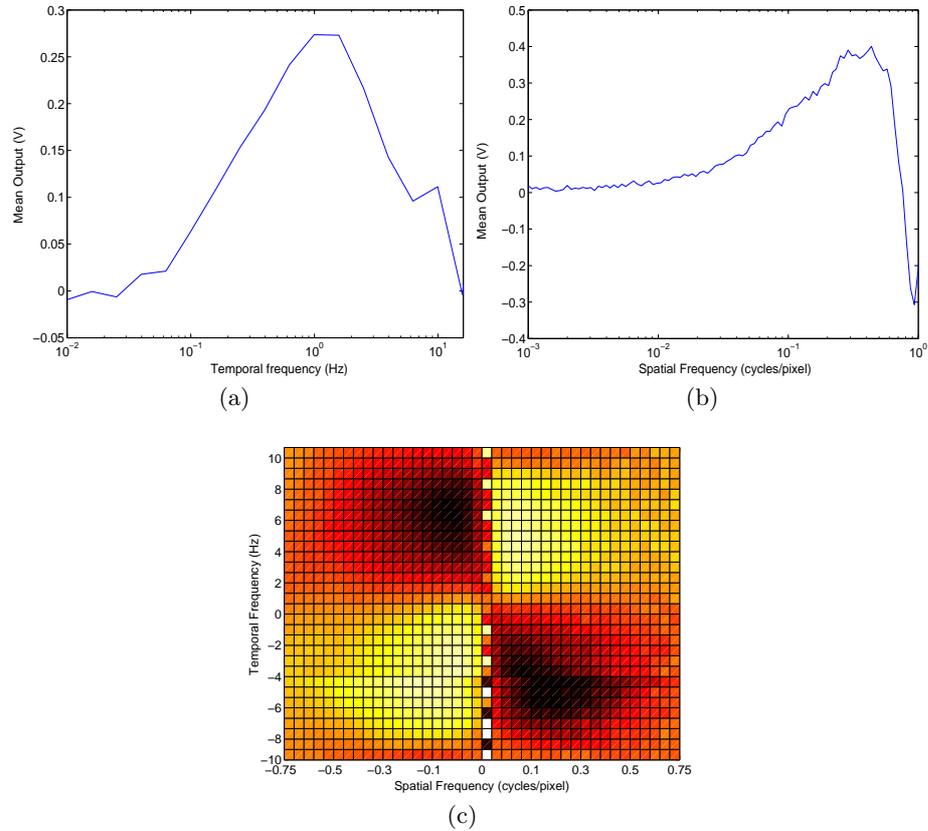


Fig. 6. Spatio-temporal frequency tuning of the sensor. (a) Temporal frequency sweep. (b) Spatial frequency sweep: note the onset of spatial aliasing. (c) Spatio-temporal frequency plot: light colors indicate positive and dark colors indicate negative average response.

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